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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,326	12/02/2003	Haining S. Yang	FIS920030318US1	3668

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EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,326	YANG, HAINING S.	
	Examiner	Art Unit	
	Hung Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-9,11-14 and 29-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,11-14 and 29-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6-8 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson et al. (PN 5,963,803, of record) in view of Sakurai et al. (US 2001/0052648, of record). Dawson et al. discloses, as shown in Figure 1L, an integrated circuit structure comprising:

first-type transistors (PFETs) and second-type transistors (NFETs) formed on a same substrate (102),

wherein the first-type transistors and the second-type transistors comprise:

gate conductors (122,126) over channel regions in the substrate;

sidewall spacers (146,144) adjacent the gate conductors;

source and drain extensions (140,142,130,132) on opposite sides of the channel regions,

wherein sidewall spacers are larger in the first-type transistors (146) than in the second-type transistors (144).

Dawson et al. discloses the claimed invention including an integrated circuit structure as recited in the rejection above. Dawson et al. does not disclose the structure further comprising silicide regions between portions of the sidewall spacers and the substrate, wherein the silicide regions

are larger in the first-type transistors than in the second-type transistors. However, Sakurai et al. discloses a structure comprising silicide regions (7b&107b,7b) between portions of sidewall spacers (9) and a substrate (1), wherein the silicide regions are larger in the first-type transistors than in the second-type transistors. Note Figure 16 of Sakurai et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the structure of Dawson et al. having silicide regions between portions of the sidewall spacers and the substrate, wherein the silicide regions are larger in the first-type transistors than in the second-type transistors, such as taught by Sakurai et al. in order to suppress occurrence of the junction leak so that an off-leak current of the transistor can be suppressed and the power consumption can be reduced.

With regard to claims 6 and 13, Dawson et al. and Sakurai et al. disclose the first-type transistors (PMOS) have different performance characteristics than the second-type transistors (NMOS).

With regard to claims 7 and 14, Dawson et al. and Sakurai et al. disclose the source and drain extensions in the first-type transistors (boron) are made of a different material than in the second-type transistors (phosphorus).

2. Claims 1-2, 4-9, 11-14 and 29-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hellig et al. (PN 6,696,334, of record) in view of Sakurai et al. (US 2001/0052648, of record).

Hellig et al. discloses, as shown in Figures 2-12, an integrated circuit structure comprising:

first-type transistors (PFETs,210,310) and second-type transistors (NFETs,215,315) formed on a same substrate (230),

wherein the first-type transistors and the second-type transistors comprise:

gate conductors (218,225,319,325) over channel regions in the substrate;

sidewall spacers (219,223,831,837) adjacent the gate conductors;

source and drain extensions (217,222,not shown) on opposite sides of the channel regions,

wherein sidewall spacers are larger in the first-type transistors than in the second-type transistors.

Hellig et al. discloses the claimed invention including an integrated circuit structure as recited in the rejection above. Hellig et al. does not disclose the structure further comprising silicide regions between portions of the sidewall spacers and the substrate, wherein the silicide regions are larger in the first-type transistors than in the second-type transistors. However, Sakurai et al. discloses a structure comprising silicide regions (7b&107b,7b)between portions of sidewall spacers (9) and a substrate (1), wherein the silicide regions are larger in the first-type transistors than in the second-type transistors. Note Figure 16 of Sakurai et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the structure of Hellig et al. having silicide regions between portions of the sidewall spacers and the substrate, wherein the silicide regions are larger in the first-type transistors than in the second-type transistors, such as taught by Sakurai et al. in order to suppress occurrence of the junction leak so that an off-leak current of the transistor can be suppressed and the power consumption can be reduced.

With regard to claims 2, 9 and 30, Hellig et al. and Sakurai et al. disclose the source and drain extensions are spaced further from the channel regions in the first-type transistors than in the second-type transistors.

With regard to claims 4 and 11, Hellig et al. and Sakurai et al. disclose the sidewall spacers include oxide liners, and wherein the oxide liners are thicker in the first-type transistors than in the second-type transistors.

With regard to claims 5, 12 and 31, Hellig et al. and Sakurai et al. disclose sidewall spacers comprise multiple-layer sidewall spacers, and sidewall spacers in the first-type transistors have more sidewall spacer layers than in the second-type transistors [Figure 12].

With regard to claims 6, 13 and 32, Hellig et al. and Sakurai et al. disclose the first-type transistors (PMOS) have different performance characteristics than the second-type transistors (NMOS).

With regard to claims 7, 14 and 33, Hellig et al. and Sakurai et al. disclose the source and drain extensions in the first-type transistors (boron) are made of a different material than in the second-type transistors (phosphorus).

With regard to claim 29, Hellig et al. discloses, as shown in Figures 2-12, an integrated circuit structure comprising:

first-type transistors (PFETs,210,310) and second-type transistors (NFETs,215,315) formed on a same substrate (230),

wherein the first-type transistors and the second-type transistors comprise:

gate conductors (218,225,319,325) over channel regions in the substrate;

sidewall spacers (219,223,831,837) adjacent the gate conductors;

source and drain extensions (217,222,not shown) on opposite sides of the channel regions,

wherein sidewall spacers include oxide liners.

Hellig et al. does not disclose the structure comprising silicide regions between portions of the sidewall spacers and the substrate, wherein the silicide regions are larger in the first-type transistors than in the second-type transistors. However, Sakurai et al. discloses a structure comprising silicide regions (7b&107b,7b) between portions of sidewall spacers (9) and a substrate (1), wherein the silicide regions are larger in the first-type transistors than in the second-type transistors. Note Figure 16 of Sakurai et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the structure of Hellig et al. having silicide regions between portions of the sidewall spacers and the substrate, wherein the silicide regions are larger in the first-type transistors than in the second-type transistors, such as taught by Sakurai et al. in order to suppress occurrence of the junction leak so that an off-leak current of the transistor can be suppressed and the power consumption can be reduced.

Note that the term "a size of said silicide regions is modulated by a thickness of said oxide liners" is method recitation in a device claimed. "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Response to Arguments

3. Applicant's arguments filed 11/16/04 have been fully considered but they are not persuasive.

It is argued, at page 9 of the Remarks, that Sakurai does not disclose silicide regions between portions of the sidewall spacers and the substrate. This argument is not convincing because Sakurai discloses, as shown in Figure 16, silicide regions (7b,107b) between portions of the sidewall spacers (9) and the substrate (1) and therefore, Sakurai's device anticipates the claimed invention. Drawings and pictures can be anticipate if they clearly show the structure which is claimed. In re Marz, 173 USPQ 25 (CCPA 1972). When the reference is a utility patent, it does not matter that the feature shown is unintended or unexplained in the specification. The drawing must be evaluated for what they reasonably disclose and suggest to one of ordinary skill in the art. In re Aslanian, 200 USPQ 500 (CCPA 1970). See MPEP 2121.04 for more information on prior art drawings as "enabled disclosures."

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

February 1, 2005

Hung Vu

Primary Examiner